**Amendments to the Claims**:

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims**:

1. (currently amended) A semiconductor device comprising:

an insulator;

a semiconductor fin formed on the insulator;

a source region adjacent a first end of the fin formed on the insulator;

a drain region adjacent a second end of the fin formed on the insulator;

a first sidewall spacer formed adjacent a first side of the fin, the first sidewall spacer having a substantially triangular shaped cross-section;

a second sidewall spacer formed adjacent a second side of the fin, the second sidewall spacer having a substantially triangular shaped cross-section; and

a gate formed over the fin and the first and second sidewall spacers, and in contact with the first and second sidewall spacers, in a channel region of the semiconductor device,

wherein the first and second sidewall spacers are formed to a width ranging from about 150 Å to about 1000 Å and wherein the first and second sidewall spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers to reduce micromasking effects during etching of the gate.

2. (canceled)

3. (original) The semiconductor device of claim 1, wherein the first and second sidewall spacers slope away from the fin.

4. (original) The semiconductor device of claim 1, wherein the gate includes an electrode portion formed away from the fin.

5. (canceled)

6. (original) The semiconductor device of claim 1, wherein the first and second sidewall spacers are formed of polysilicon.

7. (original) The semiconductor device of claim 6, wherein the gate comprises polysilicon.

Claims 8-15 (canceled)

16. (currently amended) A FinFET device comprising:

an insulator;

a semiconductor fin formed on the insulator;

a source region connected to a first end of the fin and formed on the insulator;

a drain region connected to a second end of the fin and formed on the insulator;

a first sidewall spacer formed adjacent a first side of the fin in a roughly triangular shape;

a second sidewall spacer formed adjacent a second side of the fin in a roughly triangular shape; and

a gate formed over the fin, the first sidewall spacer, and the second sidewall spacer, and

in contact with the first and second sidewall spacers, in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers and the first and second sidewall spacers reduce micromasking effects during etching of a gate material to form the gate,

wherein the first and second sidewall spacers are formed to a width of about 150 Å to about 1000 Å.

17. (canceled)

18. (original) The FinFET device of claim 16, wherein the first and second sidewall spacers slope away from the fin.

19. (canceled)